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Amendments to the Specification

Please replace the paragraph at page 2, lines 19-22 with the following amended paragraph:

Fig. 2 shows a perspective view of the light emitting thyristor matrix array circuit shown in Fig. 1, rearranged to illustrate the problem addressed by the subject invention. It is recognized from the figure that wirings L2, L4, ... from the gate electrodes g2, g4, ... are intersected with the gate-selecting ling G1.

Please replace the paragraph at page 2, lines 23-29 with the following amended paragraph:

Fig. 3 is a plan view of the light-emitting thyristor matrix array including bonding pads provided on both sides of an array of thyristors which also illustrates the problem addressed by the subject invention. In the Figure, BP(A1), BP(A2), BP(A3), ... designate the bonding pats for the ~~terminal~~ terminals A1, A2, A3, ..., and PB(G1), BP(g2) for the gate-selecting lines G1 and G2. Also, B1, B2, B3, ... denote blocks each including two contiguous light-emitting thyristors.

Please replace the paragraph at page 2, line 30 through page 3, line 4 with the following amended paragraph:

Figs. 4 and 5 show examples in which bonding pads are provided on one side of an array of thyristors and which further illustrate the problem addressed by the subject invention. In Fig. 4, bonding pads are provided on the opposite side to the gate selecting lines. In Fig. 5, bonding pads are provided on the side of the gate selecting lines.